

**INFORMATION DISCLOSURE CITATION**  
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Docket Number (Optional)

13688

Application Number

Applicant(s)

Richard S. NORMAN et al.

Filing Date

6-1-01

Group Art Unit

JC922 U.S. PRO  
09/870766



**U.S. PATENT DOCUMENTS**

*EXAMINER INITIAL	REF	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
fu	1.	U.S. 5,008,878	16/04/1991	Ahmadi et al.			
fu	2.	U.S. Re. 34,755	11/10/1994	Eng et al.			
fu	3.	U.S. Re. 34,811	27/12/1994	Eng et al.			
fu	4.	U.S. 5,361,257	01/11/1994	Petersen			
fu	5.	U.S. 5,467,347	14/11/1995	Petersen			
fu	6.	U.S. 5,999,527	07/12/1999	Petersen			
fu	7.	U.S. 5,787,084	28/07/1998	Hoang et al.			
fu	8.	U.S. 5,043,980	27/08/1991	Day, Jr. et al.			
fu	9.	U.S. 6,144,662	07/11/2000	Colmant et al.			
fu	10.	U.S. 5,938,736	17/08/1999	Muller et al.			
fu	11.	U.S. 5,247,513	21/09/1993	Henrion et al.			

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	REF	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	Translation	
							YES	NO
	12.	EP 0 680 173 A1	02/11/1995	EUROPE				

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fu	13.	Nick McKeown et al. "The Tiny Tera: a Packet Switch Core"; Departments of Electrical Engineering and Computer Science, Stanford University; August 1996; <a href="http://tiny-tera.stanford.edu/tiny-tera/index.html">http://tiny-tera.stanford.edu/tiny-tera/index.html</a>						

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fu jz

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11/26/04

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ATTY DOCKET NO.

13688-7-2

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APPLICANT(S)

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FILING DATE

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GROUP

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*EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
fu	14.	U.S. 6,111,856	29/08/2000	Huterer et al.			
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							YES	NO

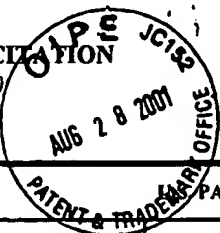
## OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)


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Docket Number (Optional) <b>13688</b>	Application Number <b>09/870,766</b>
Applicant(s) <b>Richard NORMAN et al.</b>	
Filing Date <b>June 1, 2001</b>	Group Art Unit <b>2661</b>

**PATENT DOCUMENTS**

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fr	2.	U.S. 5,072,366	10/12/1991	Simcoe			
fr	3.	U.S. 4,955,020	04/09/1990	Stone et al.			

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**AUG 31 2001**  
**Technology Center 2600**

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fr	4.	French, R., Architectural Consideration for Internet Routers; retrieved from the internet guideline in file; Internet URL <a href="http://www.cise.ufl.edu/~rfrench">www.cise.ufl.edu/~rfrench</a> , accessed July 23, 2001;
fr	5.	Joseph Desposito; Router-On-A-Chip Manages Network Traffic with Wire-Speed QoS; Electronic Design; May 1, 2000; pp 64-65-66;

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6.	Werner Bux et al.; Technologies and Building Blocks for Fast Packet Forwarding; IEEE Communications Magazine; January 2001; pp. 70-77.
7.	Minagawa, N. et al. ; Dept. of Comput. Scil, University of Electro-Commun. Tokyo, Japan; Implementation of a network switch on chips;(Abstract) Communications, vol. 13, no. 1; retrieved on March 16, 2001 from INSPEC database.
8.	Saturn: a terabit packet switch using dual round-robin; (abstract) Globecom'00 - IEEE, Global Telecommunications Conference; Dept. of Electr. Eng. Polytech, Univ. of Brooklyn, NY, U.S.A.; retrieved on June 4, 2001 from INSPEC database.
9.	Nanette J. Boden et al.; Myrinet - Gigabit-per-Second Local-Area Network [on line]; November 16, 1994 Myricom, Inc.; Internet URL <a href="http://www.myrinet.com/research/publications/Hot.ps">http://www.myrinet.com/research/publications/Hot.ps</a> ; retrieved on March 14, 2001;
10.	Vitesse Semiconductor Corporation [on line] ; Datasheet VSC880; January 5, 2001; pp. 1-20; retrieved on July 23, 2001; Internet URL <a href="http://www.vitesse.com/products/documents.cfm?family=document-id=180">www.vitesse.com/products/documents.cfm?family=document-id=180</a> ;
11.	Vitesse Semiconductor Corporation [on line] ; Datasheet VSC870; June 29, 2001; pp. 1-40; retrieved July 23, 2001; Internet URL <a href="http://www.vitesse.com">www.vitesse.com</a>
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14.	Cyrel Minkenberg et al. A combined Input and Output Queued Packet-Switched System Based on Prisma Switch-on-a-Chip Technology; Scalable High-Speed Switches/Routers with QoS Support; IBM Research, Zurich Research Laboratory; IEEE Communications Magazine; December 2000; pp 70-84;
15.	Werner Bux et al.; Technologies and Building Blocks for Fast Packet Forwarding; Telecommunications Networking at the Start of the 21st Century; IEEE Communications Magazine; January 2001; pp 70-77;
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17.	PSID - Based Communications Switching [on line] ; December 1997; Internet URL <a href="http://www.lcube.com/commsw.pdf">http://www.lcube.com/commsw.pdf</a> ; retrieved on March 15, 2001; pp 1-14

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**13688**

**09/870,766**

**Applicant(s)**

**Richard S. Norman et al.**

Filing Date

06/01/2001

### Group Art Unit

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REF	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	Translation	
						YES	NO


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	1.	WO 98/26539	06-18-1998	International				
	2.	EP 1 051 001 A2	11-08-2000	Europe				

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	3.	Partial International Search; PCT/CA02/00810

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**2661**

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fr	1.	U.S. 5,790,539	08-04-1998	Chao et al.			
fr	2.	U.S. 5,831,980	11-03-1998	Varma et al.			
	3.	U.S. 6,069,895	05-30-2000	Ayandeh			

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							YES	NO
	4.	EP 0 241 152 A2	10-14-1987	EUROPE				

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fr	5.	NOTANI H ET AL: "An 8*8 ATM switch LSI with shared multi-buffer architecture" PROCEEDINGS OF THE SYMPOSIUM ON VLSI CIRCUITS. SEATTLE, JUNE 4-6, 1992, SYMPOSIUM ON VLSI CIRCUITS, NEW YORK, IEEE, US, 4 June 1992 (1992-06-04), pages 74-75, XP010064987						
fr	6.	International Search Report PCT/CA02/00810, August 1, 2003						

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